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(54) Selective repeat ARQ protocol on virtual circuits

(57) The present invention concerns a method of controlling errors in packets transmitted over at least one transmission link between a transmitter and a receiver, said transmitter receiving from an input multiplex packets belonging to a plurality of virtual circuits and transmitting them in the form of sequences of packets over a or said transmission line, said receiver, on reception of a packet, checking whether it is in the order of the sequence or out of life time and if so, delivering it to an output multiplex, and if not, sending to the said transmitter a negative acknowledgement of the packet or packets which have been lost in order to have it or them retransmitted.

According to the invention, at the transmitter side, two indexes are allocated to each packet to be transmitted over the transmission line, one index indicating the sequence number of the packet to be transmitted and the other index has a value amongst at least two specific values, one value meaning that no resequencing is needed and the other (or the others) respectively meaning that the difference between the sequence number of the packet to be transmitted and the previous packet of the same virtual circuit is larger than a predetermined value (or predetermined values), and, at the receiver side, on receipt of a packet corresponding to the one expected, a pointed packet is determined which sequence number is given by the difference between the sequence number of said received packet and the predetermined value represented by the second index carried by said received packet, and if said pointed packet and all packets sent by the transmitter before have already been correctly received by the receiver and delivered to the output multiplex or have been discarded by the life time, said received packet is delivered

to the output multiplex, and if it is not the case, said received packet will be retained until the pointed packet and all the packets before will be delivered or discarded by the life time.

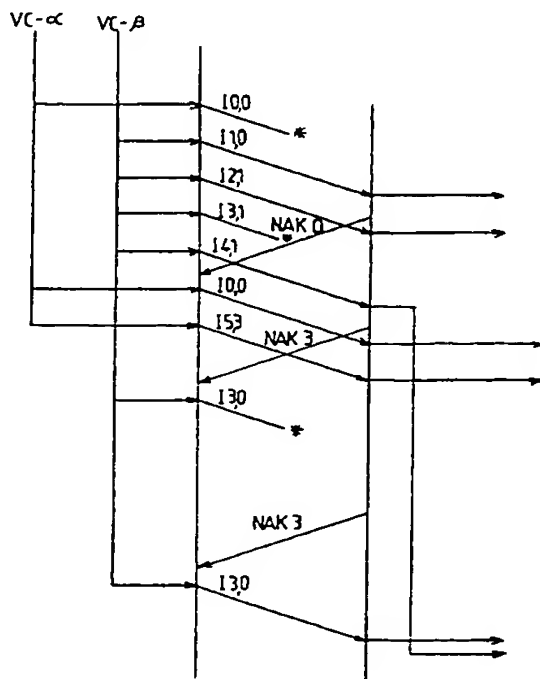


FIG. 3

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Description

[0001] The present invention concerns a method of controlling errors in packets transmitted on at least one transmission link between a transmitter and a receiver. The present invention applies essentially in cases where the said link can support a plurality of virtual circuits.

[0002] The present invention applies to a transmission system of the type depicted in Fig. 1. In this Fig. 1, a transmitter 10 can be seen which receives, from an input multiplex 11, packets which may belong to several different virtual circuits. This transmitter 10 transmits, to a receiver 30 via a transmission line 20, the packets which it receives from the multiplex 11, in the form of sequences of packets. On receiving the packets from the transmission line 20, the receiver 30 implements a method of controlling errors which takes place during the transmission. More particularly, the packets received in the order of the sequence are delivered to an output multiplex 31. But, if the packet received does not have the expected sequence number notably because of a loss of one or more packets, it is not delivered to the output multiplex 31 as long as the lost packet or packets have not been received or as long as the maximum waiting time has not expired.

[0003] An implementation of a such a method is illustrated in Fig. 2. The left-hand part of this Fig. 2 is a diagram showing, at the transmitter, the transmission of packets as a function of time (the time elapses downwards) and the right-hand part is a diagram showing, at the receiver, the reception of transmitted packets also as a function of time. As for the central part, this depicts the transmission of the packets over the transmission line.

[0004] Two virtual circuits VC- α and VC- β are multiplexed on the transmission line between the transmitter and receiver. Each packet transmitted over the transmission line carries a sequence number which identifies it, in the sequence of transmitted packets, with respect to the preceding ones and the following ones.

[0005] As shown in this diagram, the packet l_0 (the first packet in a sequence of packets) which belongs to the second virtual circuit VC- β has been received correctly. This packet l_0 is then delivered to the output multiplex 31.

[0006] The packet l_1 on the other hand has been lost and is therefore not received by the receiver 30. On reception of the packet l_2 , the receiver 30 notes that the sequence number in the sequence is not the one required. It is in fact 2 whereas it is the packet l_1 , and therefore with the sequence number 1, which is expected. The receiver 30 therefore sends to the transmitter 10 a negative acknowledgement NAK₁, thus requesting the transmitter 10 to re-transmit the packet l_1 .

[0007] As for the packets l_2 to l_4 , they have been correctly received by the receiver. However, because

the packet l_1 has not been correctly received, they are not delivered and are then stored whilst awaiting their delivery. It will also be said that they are retained.

[0008] After the transmission of the packet l_4 , the transmitter 10 receives the negative acknowledgement NAK₁ concerning the packet l_1 and consequently re-transmits this packet l_1 , which is received later at the receiver. As can be noted, the receiver delivers to the output multiplex not only the packet l_1 but also the packets l_2 to l_4 which had been retained up till now.

[0009] Thus, according to this known method, the packets which have been received after the loss of a packet are not delivered and are retained, until the packet is correctly received.

[0010] It is possible that the packet l_1 may not always be correctly received by the receiver 30. Conventionally, the packets l_2 , l_3 and l_4 are then delivered after the expiry of a predetermined time, referred to as the maximum waiting time.

[0011] It will be noted that such a process requires only the sequence number of sending of the packets in the current sequence in order to function correctly.

[0012] However, when several virtual circuits are multiplexed on one and the same transmission link between a transmitter and receiver, it may happen that packets belonging to one virtual circuit are retained because a packet belonging to another virtual circuit has been lost. This eventuality is also illustrated in Fig. 2, where it can be seen that the packets l_1 and l_4 belong to the same virtual circuit VC- α and that the packets l_0 , l_2 and l_3 belong to the other virtual circuit VC- β . The packets l_2 and l_3 of the virtual circuit VC- β are retained whereas, with regard to this circuit VC- α , no packet has been lost. Thus, the lost packet l_1 belonging to the virtual circuit VC- α blocks the delivery of the packets of the virtual circuit VC- β .

[0013] The aim of the present invention is therefore to resolve this problem in the case of multiplexing of several virtual circuits on the transmission link.

[0014] In order to achieve this aim, an error control method according to the invention is characterised in that, at the transmitter side, two index are allocated to each packet to be transmitted over the transmission line, one index indicating the sequence number of the packet to be transmitted and the other index has a value amongst at least two specific values, one value meaning that no resequencing is needed and the other (or the others) respectively meaning that the difference between the sequence number of the packet to be transmitted and the previous packet of the same virtual circuit is larger than a predetermined value (or predetermined values), and, at the receiver side, on receipt of a packet corresponding to the one expected, a pointed packet is determined which sequence number is given by the difference between the sequence number of said received packet and the predetermined value represented by the second index carried by said received packet, and if said pointed packet and all packets sent

by the transmitter before have already been correctly received by the receiver and delivered to the output multiplex or have been discarded by the life time, said received packet is delivered to the output multiplex, and if it is not the case, said received packet will be retained until the pointed packet and all the packets before will be delivered or discarded by the life time.

[0015] According to an advantageous characteristic of the invention, the predetermined value or the lowest predetermined value corresponding to the specific value allocated by the transmitter is equal to 1.

[0016] According to an another characteristic of the invention, the values allocated by said transmitter can furthermore take intermediary values each pointing to the previous packet of the same virtual circuit than the packet to be transmitted and, at the receiver side, when a packet carrying an intermediary value is received, the previous packet of the same virtual circuit pointed to by said intermediary value is determined, and if said previous packet has been already delivered, said received packet is delivered, and if this is not the case, said received packet is retained until the pointed packet will be delivered or discarded by the life time.

[0017] According to an advantageous characteristic, the predetermined value or the lowest predetermined value corresponding to the specific value allocated by the transmitter is equal to the largest value that can be taken by the intermediary values plus 1.

[0018] According to an another characteristic of the invention, said intermediary values allocated by the transmitter represent the difference between the sequence number of the packet to be transmitted and the sequence number of the previous packet in the same virtual circuit, and, at the receiver side, the previous packet of said received packet is determined by the difference between the sequence number of said received packet and the value represented by the second index carried by said received packet.

[0019] The above mentioned characteristics of the invention, along with others, will appear more clearly on reading the following description of several embodiments of the invention, said description being made in relation to the attached drawings, among which:

Fig. 1 is a block diagram of a transmission system to which the present invention can be applied,

Fig. 2 is a diagram illustrating an error control method in accordance with a method of the prior art,

Fig. 3 is a diagram illustrating a first implementation of an error control method according to the present invention,

Fig. 4 is a diagram illustrating a second implementation of an error control method according to the present invention,

Fig. 5 is another diagram illustrating another aspect of an error control method according to the present invention, and

Fig. 6 is a diagram illustrating a fourth implementation of an error control method according to the invention, and

Fig. 7 is a diagram illustrating a fifth implementation of an error control method according to the present invention, which is a combination of the methods depicted in Figs. 5 and 6.

[0020] According to the present invention, at the transmitter side 10, two indices i and j are allocated to each packet to be transmitted over the transmission line. The first index i represents the sequence number of the packet to be transmitted. The second index j has at least two specific values. One value, for example 0, means that no resequencing is needed. This is the case generally for the first packet of a virtual circuit. The other specific value(s) means that the difference between the sequence number i of the packet to be transmitted and the previous packet of the same virtual circuit is larger than or equal to a predetermined value a .

[0021] At the receiver side, on receipt of a packet i, j which will subsequently be referred to as the just received packet, a check is made whether its sequence number i corresponds to the one expected. If such is not the case, this means that at least one packet has been lost. A negative acknowledgement is then sent to the transmitter 10 in order to have it retransmitted.

[0022] Furthermore, if its sequence number i corresponds to the one expected, a previous packet is determined which sequence number is given by the difference $(i - a)$ between the sequence number i of the just received packet and the predetermined value a represented by the second index j .

[0023] It is then determined whether all packets sent by the transmitter before the previous packet $i_{i-a,x}$ (packet $i_{i-a,x}$ included) have already been correctly received by the receiver and delivered to the output multiplex or have been discarded by the life time.

[0024] If such is the case, the packet i, j just received is delivered to the output multiplex 31. But, if not, the packet i, j will be retained until all these packets ($i_{0,0}$ to $i_{i-a,x}$) are delivered or have been discarded by the life time.

[0025] In addition, if the packet i, j just received is a packet whose receipt is awaited, it is delivered to the output multiplex 31. Then, amongst all the retained packets, those packets that can be delivered if only this one i, j is, are delivered.

[0026] It should be noted that when only one specific value is provided, the corresponding predetermined value a must be equal to 1. When more than one specific values are provided, the lowest predetermined value a must be equal to 1.

[0027] Fig. 3 illustrates an example of implementation of an embodiment of the invention. It can be seen particularly that packets belong to two virtual circuits VC- α and VC- β of the input multiplex 11 and are transmitted over a transmission line. The first index i of each

new packet transmitted over the transmission line is incremented by one unit with respect to the previous one of the sequence. This index is zero for the first packet.

[0028] The second index is zero for the first packet in the sequence of each virtual circuit, for example packets $l_{0,0}$ of virtual circuit VC- α and $l_{1,0}$ of virtual circuit VC- β .

[0029] In the other cases, the second index represents a value which permits to point to a previous packet. For example, packet $l_{5,3}$ points to packet $l_{5-3,x} = l_{2,1}$.

[0030] It should be noted that second index j and its value a are here confused.

[0031] The previous packet of the same virtual circuit than the just received packet is either the pointed packet or a packet before the pointed packet.

[0032] For example, if we consider that $l_{5,3}$ is the just received packet, then the pointed packet is $l_{2,1}$ and we can note that the previous packet of the same virtual circuit VC- β , which is packet $l_{0,0}$, is before packet $l_{2,1}$. According to this example, packet $l_{5,3}$ is also delivered since the pointed packet $l_{2,1}$ and all the packets before, i.e. packets $l_{2,1}$, $l_{1,0}$ and $l_{0,0}$, are already delivered to the output multiplex.

[0033] If we now consider that $l_{4,1}$ is the just received packet, then the pointed packet is $l_{3,1}$ and we can note that the previous packet of the same virtual circuit VC- α is also the pointed packet $l_{3,1}$. Since packet $l_{3,1}$ is not still correctly received and then is not delivered, packet $l_{4,1}$ is retained. It will be delivered when packet $l_{3,0}$ will be correctly received.

[0034] In Fig. 4, packets $l_{0,0}$ and $l_{2,1}$ are not correctly received. If we consider packet $l_{3,1}$ is the just received packet, then the pointed packet is $l_{2,1}$ which is also the previous packet of the same virtual circuit VC- β . Since, packet $l_{2,1}$ and also packet $l_{0,0}$ are not still correctly received and then are not delivered, packet $l_{3,1}$ is retained. It will be delivered when these packets $l_{0,0}$ and $l_{2,0}$ will be correctly received after retransmission. Note that the second index is now zero and not one.

[0035] The same is for packets $l_{3,1}$, $l_{4,1}$ and $l_{5,3}$. It should be noted that packet $l_{5,3}$ is retained although packet $l_{0,0}$ which belongs to the same virtual circuit VC- α is delivered.

[0036] The advantage of the invention is that the second index can be a one-bit index. When it is zero, no packet is pointed to. When it is one, as above explained, it necessarily represents value $a = 1$ and the pointed packet has a sequence number equal to $i - 1$, where i is the sequence number of the just received packet.

[0037] According to another embodiment of the present invention, the second index j has more than two specific values. One means no packet is pointed to. Another represents a value a and the others, intermediary values, represent each a value comprised between 1 to $a - 1$. According to the present embodiment, the predetermined value a corresponding to the second

specific value must be equal to the largest value ($a - 1$) that can taken by the intermediary values plus 1.

[0038] In the example of Fig. 4, the second index can be zero, 1 to 14 ($a - 1 = 14$) and a specific value is 15 ($a = 15$).

[0039] Zero means that no resequencing is needed. This is the case generally for the first packet of a virtual circuit. Intermediary values permit to determine the previous packet of the same virtual circuit. The sequence number of that previous packet is the difference between the sequence number of the just received packet and the second index ($i - j$).

[0040] When a packet $l_{i,j}$ is just received, the previous packet $l_{i-j,x}$ is determined. If the previous packet $l_{i-j,x}$ is already delivered, then the just received packet $l_{i,j}$ is also delivered. If this is not the case, packet $l_{i,j}$ is retained.

[0041] The specific value has the same meaning as for the preceding embodiment. It permits to determine a pointed packet and the previous packet of the same virtual circuit is that pointed packet or a packet before that pointed packet. When a packet $l_{i,a}$ is just received, the previous packet $l_{i-a,x}$ is determined. If all the packets before this pointed packet $l_{i-a,x}$ are already delivered, then the just received packet $l_{i,a}$ is also delivered. If this is not the case, packet $l_{i,a}$ is retained.

[0042] An example of such an embodiment is now described in relation with Fig. 5. In this example, packet $l_{0,0}$ is not correctly received twice. This is also the case for packet $l_{17,1}$. By way of an example, packet $l_{2,1}$ points to the previous packet of the same virtual circuit, i.e. packet $l_{2-1,x} = l_{1,0}$. Also by way of an example, packet $l_{17,1}$ points to the previous packet of the same virtual circuit, i.e. packet $l_{17-1,x} = l_{16,1}$.

[0043] In Fig. 5, 15 is assumed to be the specific value, meaning that the previous packet in the same virtual circuit of the packet which second index is 15 is the pointed packet or before the pointed packet.

[0044] When packet $l_{18,15}$ is correctly received, the pointed packet is determined. It is packet $l_{18-15,x} = l_{3,1}$. The previous packet in the same virtual circuit of packet $l_{18,15}$ is before $l_{3,1}$ since it is packet $l_{0,0}$. In the case represented in Fig. 5, packet $l_{18,15}$ is delivered since, when it is received, all packets before the pointed packet $l_{3,1}$ are delivered.

[0045] An example of another embodiment is depicted in relation to Fig. 6.

[0046] According to that embodiment, the second index can have more than two values. The first is zero meaning that no resequencing is needed. The others represent different predetermined values a_1 to a_n . According to the present embodiment, the lowest predetermined value must be equal to 1. As above, the second index means that the previous packet in the same virtual circuit of a considered packet has a sequence number lower or equal to the sequence number of a pointed packet which sequence number is equal to the difference between the sequence number of the consid-

ered packet and the value represented by the second index of that packet. In other words, the difference between the sequence numbers of the considered packet and of the previous packet in the same virtual circuit is larger than or equal to the value represented by the second index.

[0047] But according to this example, more than one value can be used.

[0048] In Fig. 6, the second index can take four values. The first is zero meaning that no resequencing is needed. The second means that the difference between the sequence numbers of the considered packet and of the previous packet in the same virtual circuit is larger than or equal to one. The third means that the difference is larger or equal to 17 and the fourth that the difference is larger than or equal to, for example, 65.

[0049] It should be noted that such a second index can be a two bits code.

[0050] In this Fig. 6, packet $l_{1,0}$ is delivered without any resequencing delay, since its second index is zero. As for packets $l_{2,1}$ to $l_{15,1}$, their second index represent value 1 (note that the second index and its represented value are here confined). They are delivered without any resequencing since all previous packets have been delivered. Packet $l_{16,1}$ is lost and retransmitted and packets $l_{17,1}$ and $l_{18,1}$ which respectively point to packet $l_{16,1}$ and packet $l_{17,1}$ are retained by the receiver in order to wait the correct reception of the retransmitted packet $l_{16,x}$.

[0051] As for packet $l_{19,2}$, it points to packet $l_{19-17,x} = l_{2,1}$ that means the previous packet in the same virtual circuit is that pointed packet or before. In that case, it is the pointed packet $l_{2,1}$. Since this pointed packet $l_{2,1}$ and all the packets before (here only packet $l_{1,0}$) are delivered when packet $l_{19,2}$ is received, packet $l_{19,2}$ is delivered.

[0052] Packets $l_{20,1}$ to $l_{23,1}$ including packet $l_{21,1}$ (which don't belong to the same virtual circuit) are retained by the receiver in order to wait for the correct reception of the retransmitted packet $l_{16,x}$.

[0053] Packet $l_{24,1}$ is delivered since all previous packets in the sequence have been delivered.

[0054] Fig. 7 is another example of an embodiment of the invention combining the embodiments of Fig. 5 and the one of Fig. 6.

[0055] In such an embodiment, the second index can have n values. First, for example zero, means that no resequencing is needed. $(n - m - 1)$ values are used for pointing to the previous packet in the same virtual circuit than the considered packet. Each value represents the difference of the sequence numbers of the considered packet and the previous packet in the same virtual circuit. The last m values represent predetermined values a_1 to a_m , the difference between the sequence number of the considered packet and the sequence number of the previous packet in the same virtual packet being larger than the value a_i represented by the second index. According to the present

embodiment, the lowest predetermined value a_1 must be equal to the largest value that can be taken by the intermediary values plus one.

[0056] According the example depicted in Fig. 7, the second index can take the following values :

- 0, meaning that non resequencing is needed,
- 1 to 12 representing the offset to the previous packet of the same virtual circuit,
- 13 meaning that the difference between the sequence numbers of the considered packet and the previous one of the same virtual circuit is larger than 13,
- 14 meaning that the difference is larger than 31, and
- 15 meaning that the difference is larger than 63.

[0057] It should be noted that these values can be 4 bits values and can be applied for 7 bits sequence numbers.

[0058] In Fig. 7, packet $l_{1,0}$ is delivered since its second index is zero. Packets $l_{2,1}$ to $l_{5,1}$ points to the immediately previous packet. Since each previous packet has been delivered, these packets $l_{2,1}$ to $l_{5,1}$ are also delivered. Packet $l_{16,1}$ is lost and will be retransmitted. Packets $l_{17,1}$ and $l_{18,1}$ are retained since packet $l_{16,1}$ has not been correctly received.

[0059] The previous packet of packet $l_{19,13}$ in the same virtual circuit is packet $l_{2,1}$. The sequence numbers offset is 17 which is larger than 13 but lower than 31. So, its second index, which is allocated at the emitter side, is 13. Since, at the receiver side, all the packets (here only packets $l_{2,1}$ and $l_{1,0}$) before packet $l_{2,1}$ (this one included) are delivered, packet $l_{19,13}$ is also delivered.

[0060] Packet $l_{20,2}$ is retained since the previous packet $l_{18,1}$ in the same virtual circuit has been retained.

[0061] Packet $l_{21,2}$ is delivered since packet $l_{19,x}$ has been delivered. Packets $l_{22,2}$ and $l_{23,1}$ are retained due to the resequencing.

[0062] When packet $l_{16,0}$ which has been retransmitted is correctly received, all the packets retained that either directly or indirectly points this one are delivered.

[0063] Packet $l_{24,3}$ is delivered since the pointed packet $l_{21,x}$ has been previously delivered.

Claims

1. A method of controlling errors in packets transmitted over at least one transmission link between a transmitter and a receiver, said transmitter receiving from an input multiplex packets belonging to a plurality of virtual circuits and transmitting them in the form of sequences of packets over a or said transmission line, said receiver, on reception of a packet, checking whether it is in the order of the sequence or out of life time and if so, delivering it to an output multiplex, and if not, sending to the said

transmitter a negative acknowledgement of the packet or packets which have been lost in order to have it or them retransmitted, wherein, at the transmitter side, two index are allocated to each packet to be transmitted over the transmission line, one index indicating the sequence number of the packet to be transmitted and the other index has a value amongst at least two specific values, one value meaning that no resequencing is needed and the other (or the others) respectively meaning that the difference between the sequence number of the packet to be transmitted and the previous packet of the same virtual circuit is larger than a predetermined value (or predetermined values), and, at the receiver side, on receipt of a packet corresponding to the one expected, a pointed packet is determined which sequence number is given by the difference between the sequence number of said received packet and the predetermined value represented by the second index carried by said received packet, and if said pointed packet and all packets sent by the transmitter before have already been correctly received by the receiver and delivered to the output multiplex or have been discarded by the life time, said received packet is delivered to the output multiplex, and if it is not the case, said received packet will be retained until the pointed packet and all the packets before will be delivered or discarded by the life time.

2. A method according to claim 1, wherein the predetermined value or the lowest predetermined value corresponding to the specific value allocated by the transmitter is equal to 1.
3. A method according to claim 1, wherein the values allocated by said transmitter can furthermore take intermediary values each pointing to the previous packet of the same virtual circuit than the packet to be transmitted and, at the receiver side, when a packet carrying an intermediary value is received, the previous packet of the same virtual circuit pointed to by said intermediary value is determined, and if said previous packet has been already delivered, said received packet is delivered, and if this is not the case, said received packet is retained until the pointed packet will be delivered or discarded by the life time.
4. A method according to claim 3, wherein the predetermined value or the lowest predetermined value corresponding to the specific value allocated by the transmitter is equal to the largest value that can be taken by the intermediary values plus 1.
5. A method according to claim 2, 3 or 4, wherein said intermediary values allocated by the transmitter represent the difference between the sequence

number of the packet to be transmitted and the sequence number of the previous packet in the same virtual circuit, and, at the receiver side, the previous packet of said received packet is determined by the difference between the sequence number of said received packet and the value represented by the second index carried by said received packet.

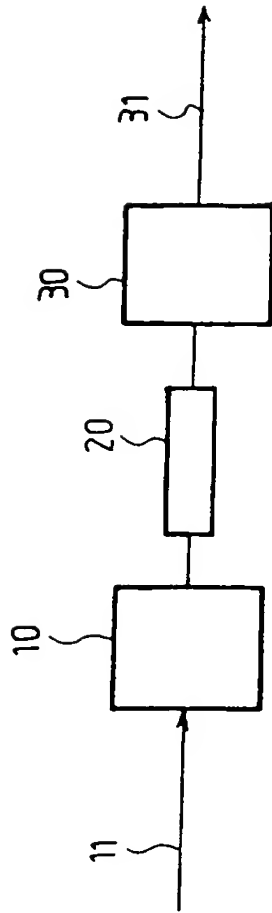


FIG. 1

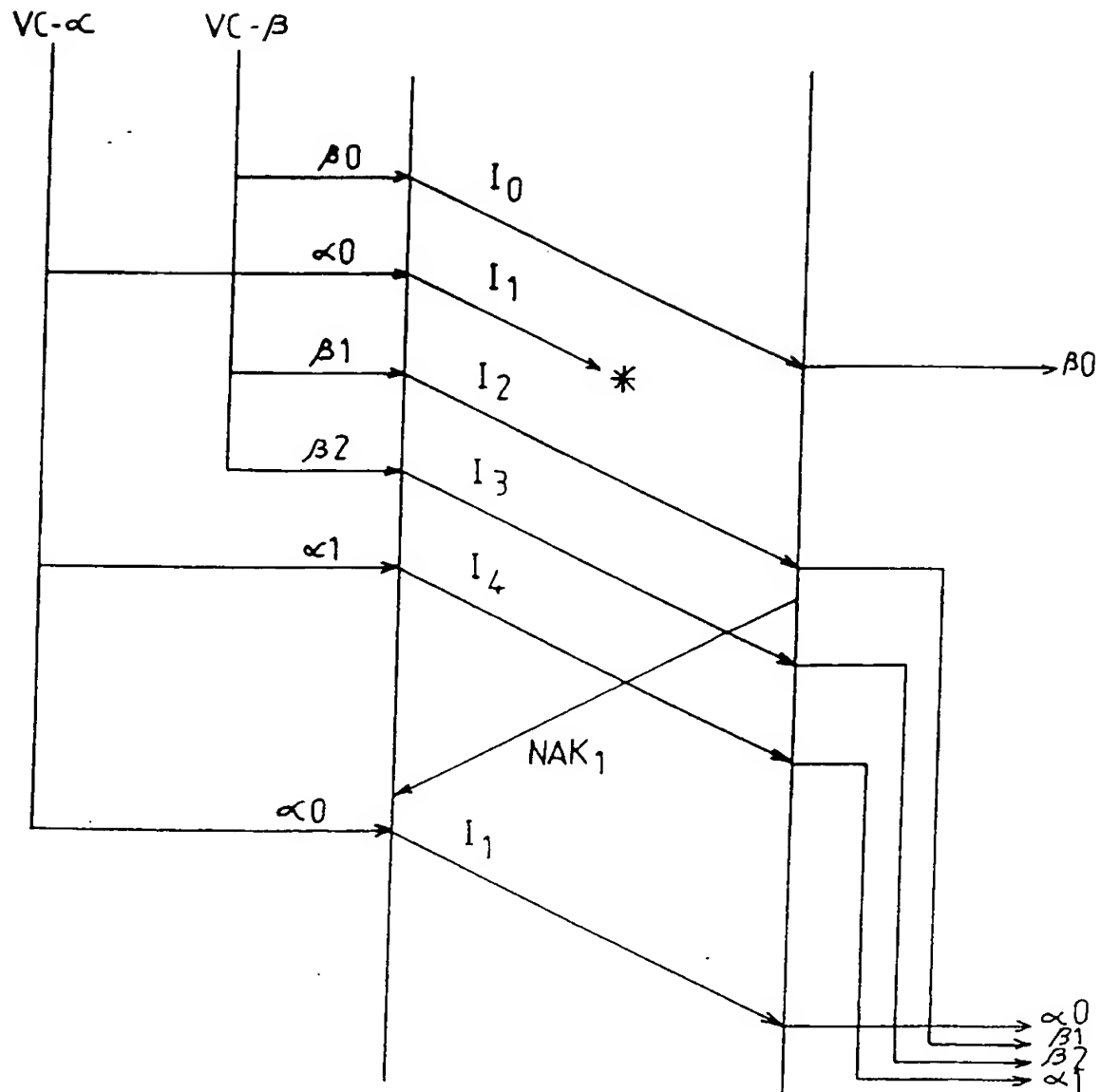
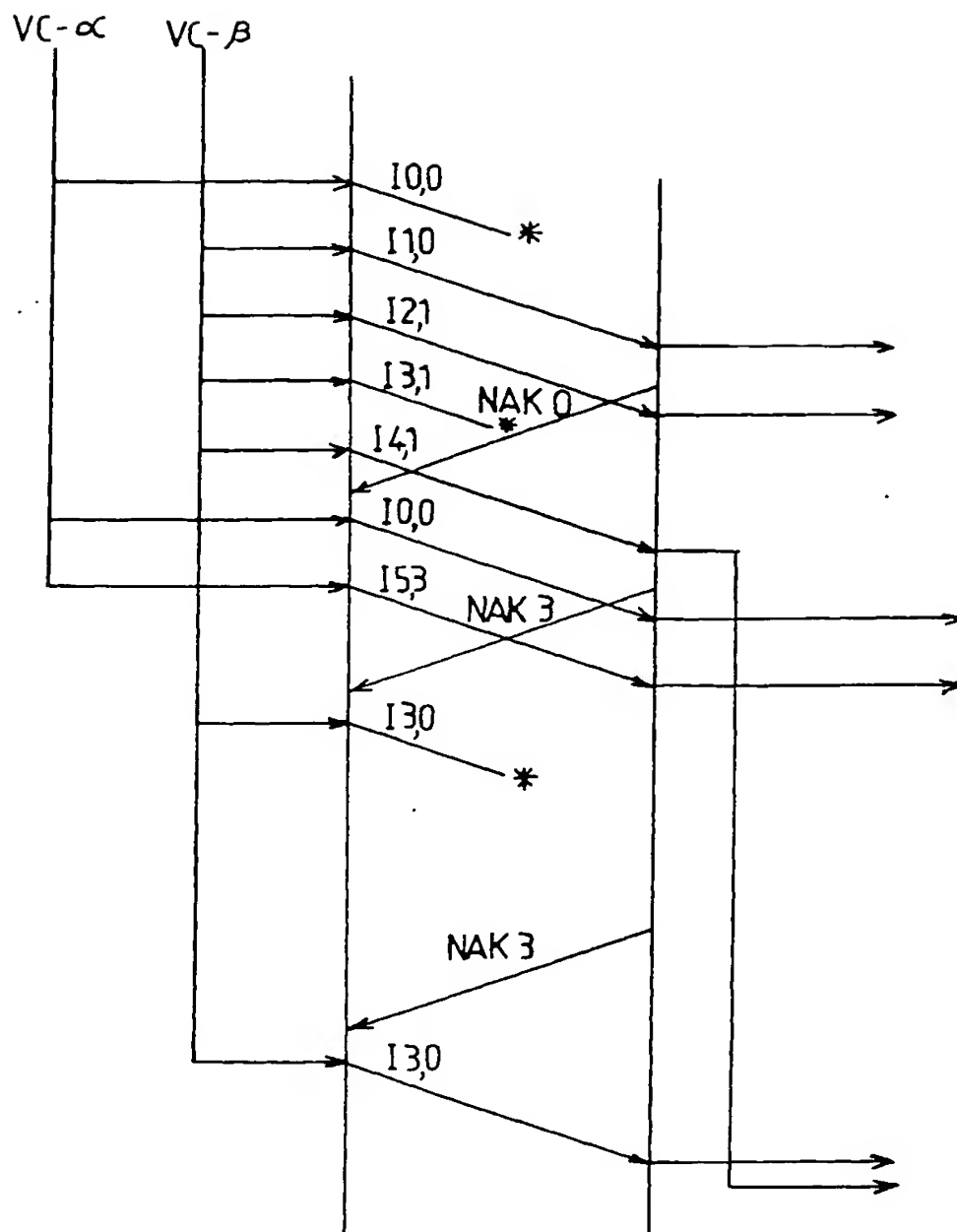


FIG. 2

FIG. 3

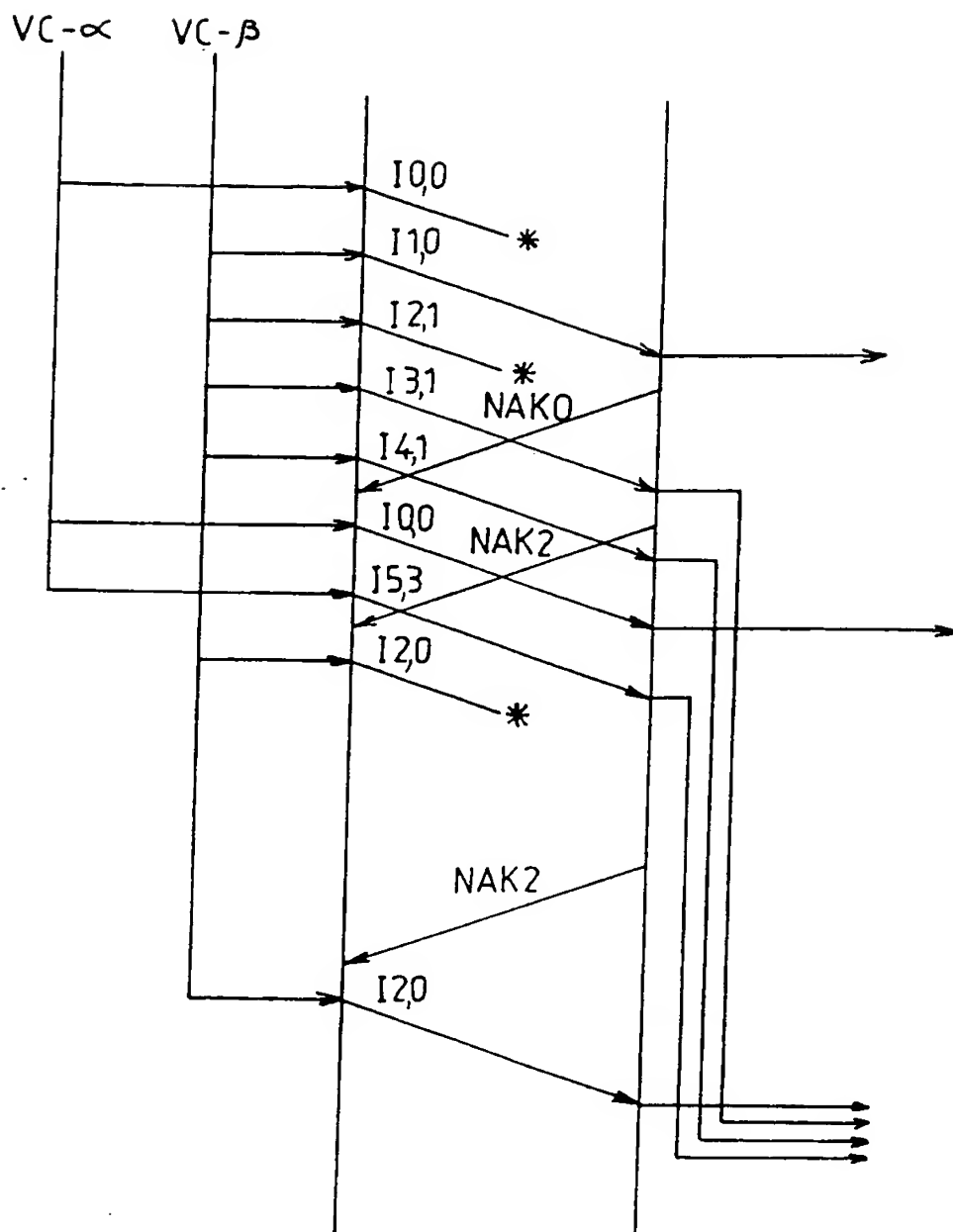


FIG. 4

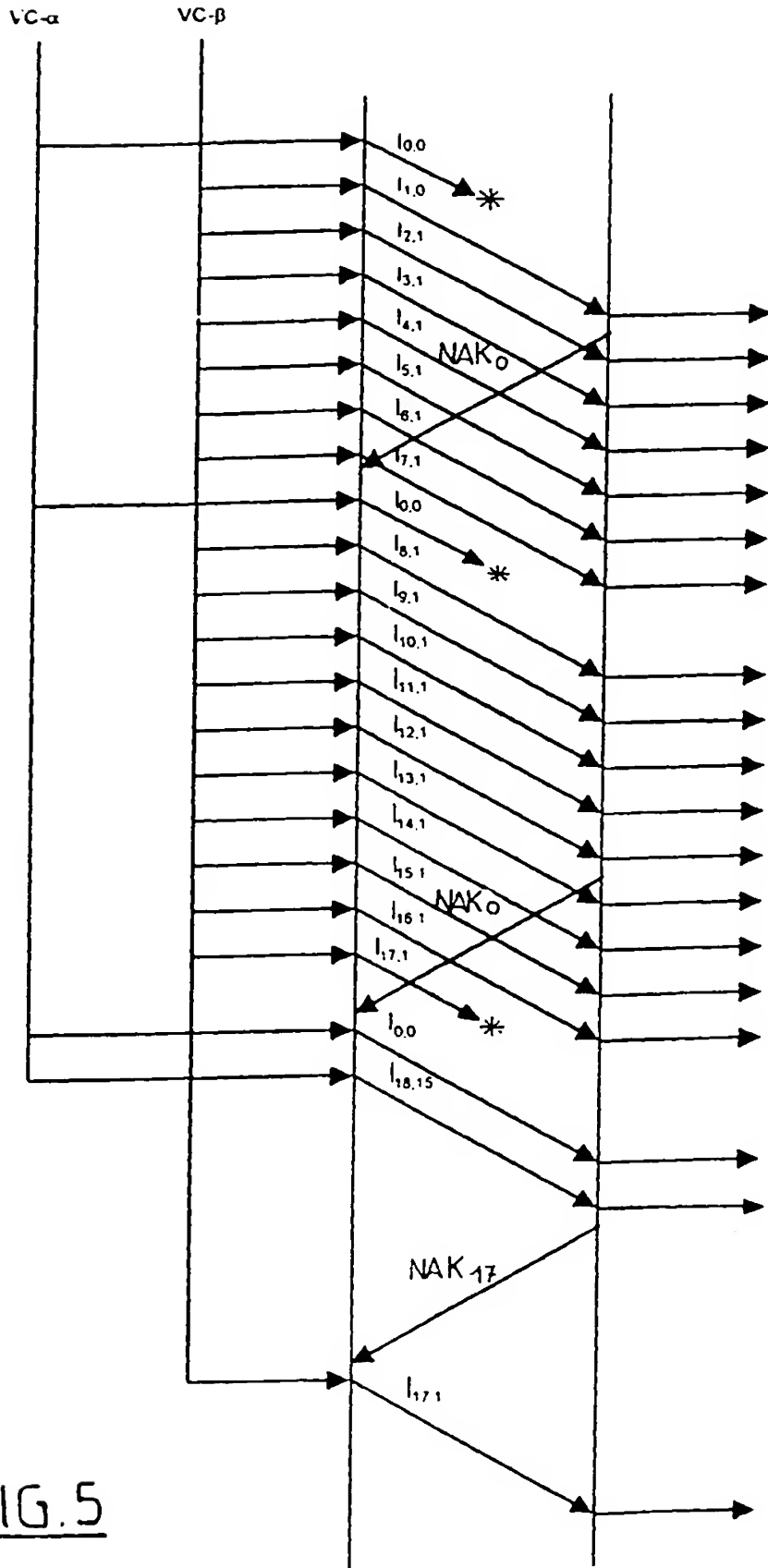


FIG. 5

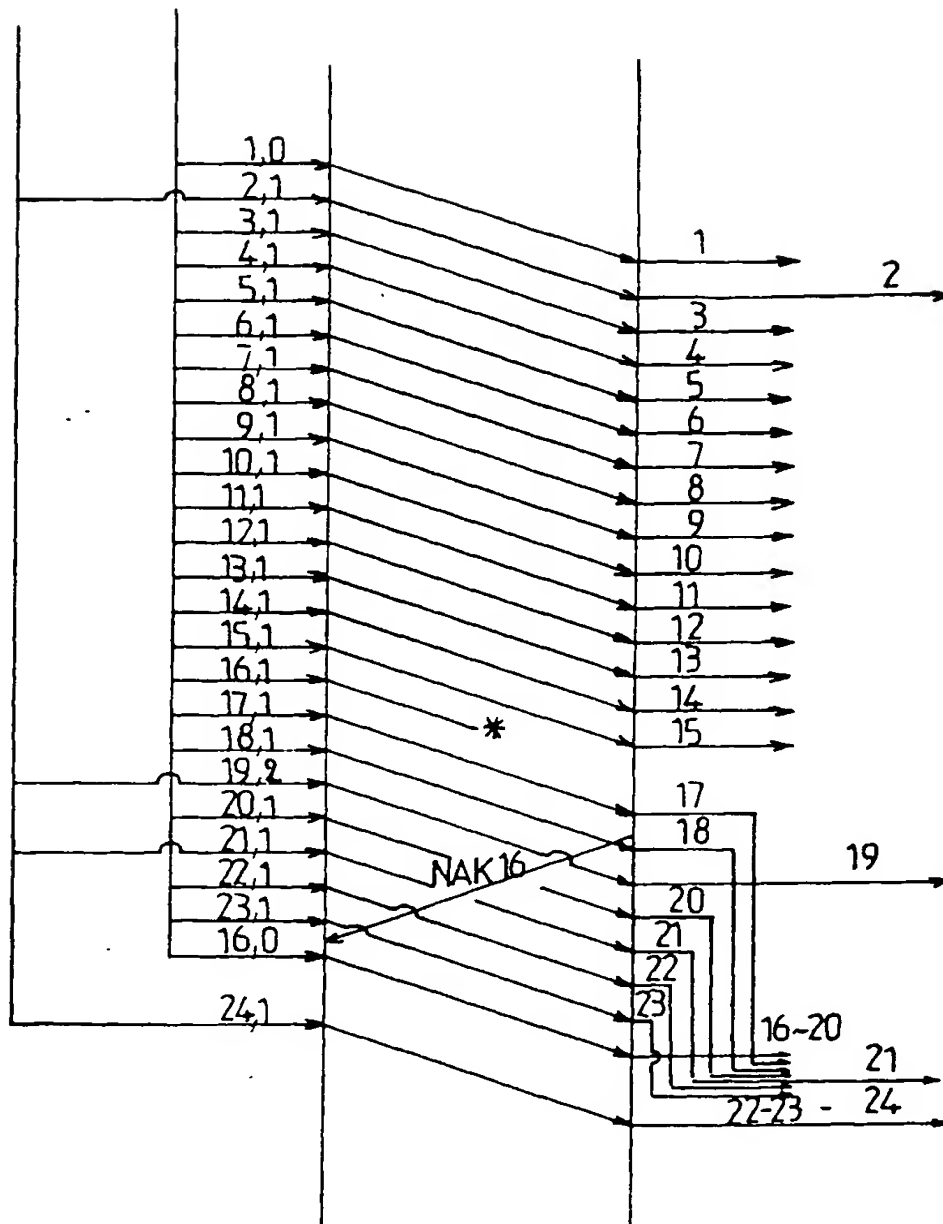


FIG. 6

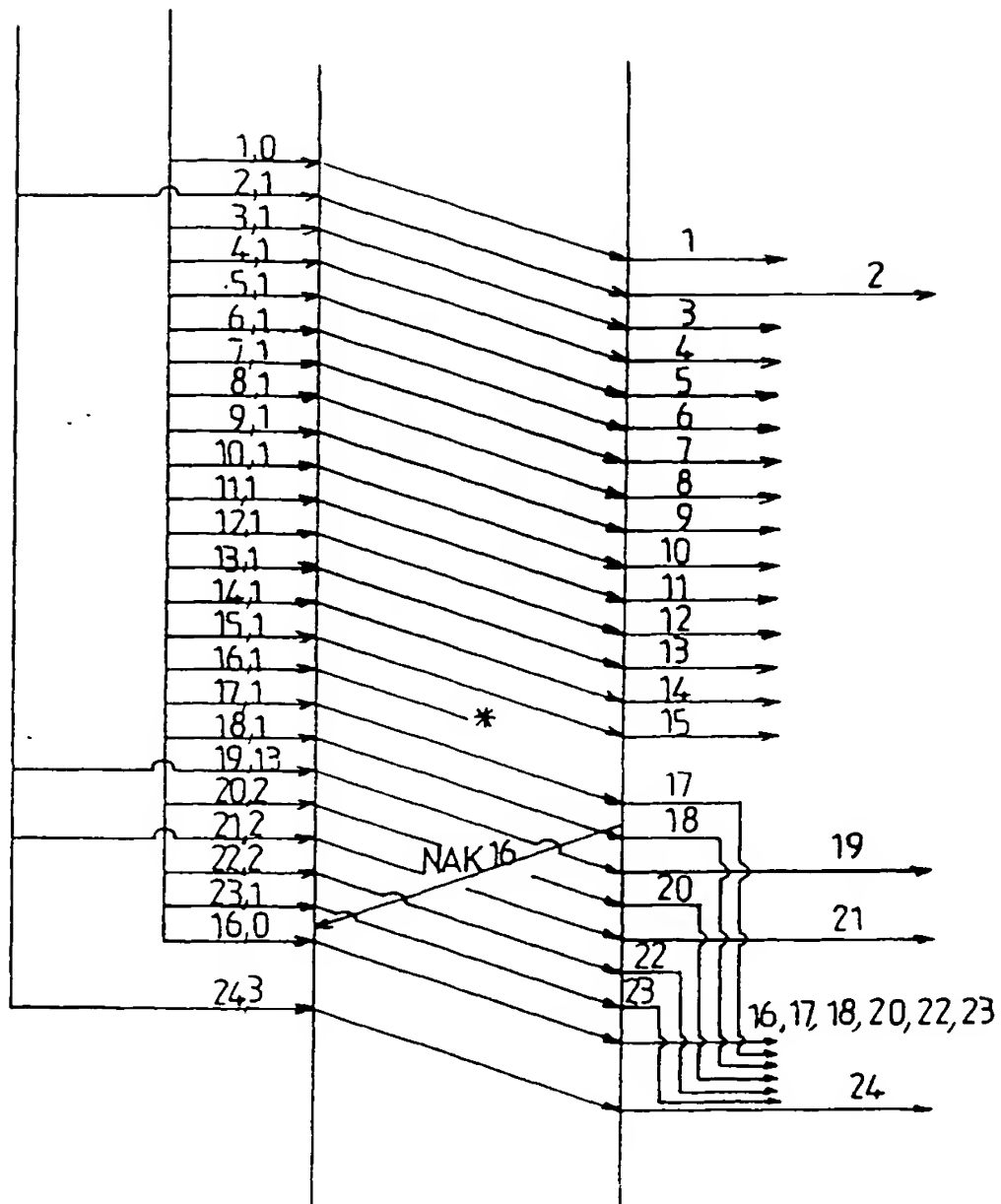


FIG. 7



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 98 40 2594

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IntCL6)
A	EP 0 193 091 A (HITACHI LTD) 3 September 1986 * the whole document *	1	H04L1/18
A	LEUNG C H C ET AL: "A NEW EFFICIENT ARQ SCHEME FOR SATELLITE COMMUNICATIONS" COMPUTER NETWORKS AND ISDN SYSTEMS, vol. 23, no. 4, January 1992, pages 229-240, XP000246519 Amsterdam, NL * section 2 * * figures 1-4 *	1	
A	NACHUM SHACHAM ET AL: "A SELECTIVE-REPEAT-ARQ PROTOCOL FOR PARALLEL CHANNELS AND ITS RESEQUENCING ANALYSIS" IEEE TRANSACTIONS ON COMMUNICATIONS, vol. 40, no. 4, April 1992, pages 773-782, XP000297814 New York, US * sections I-II *	1	
A	NACHUN SHACHAM ET AL: "A SELECTIVE REPEAT ARQ PROTOCOL FOR PARALLEL CHANNELS AND ITS RESEQUENCING ANALYSIS" COMPUTER COMMUNICATION TECHNOLOGIES FOR THE 90'S, no. 9, 30 October 1988 - 3 November 1998, pages 259-264, XP000077386 Tel Aviv, Israel * sections 1-2 *	1	
			TECHNICAL FIELDS SEARCHED (IntCL6)
			H04L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 26 March 1999	Examiner De Riccardis, F
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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL.6)
A	SHACHAM N ET AL: "RESEQUENCING DELAY AND BUFFER OCCUPANCY IN SELECTIVE REPEAT ARQ WITH MULTIPLE RECEIVERS" IEEE INFOCOM '88: NETWORKS. EVOLUTION OR REVOLUTION?, no. 7, 27 - 31 March 1988, pages 515-524, XP000014061 New Orleans, LA, USA * sections 1-2 *	1	
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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. CL.6)
Place of search THE HAGUE		Date of completion of the search 26 March 1999	Examiner De Riccardis, F
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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